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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPLICATION	FILING DATE	CLASS	SUBCLASS	GROUP ART UNIT	EXAMINER
10026950	12/27/2001	428	397	315	BROCK

**APPLICANTS: Yaegashi Seiji; Kotani Kenji; Yanagisawa Masaki; Yano Hiroshi;

**CONTINUING DATA VERIFIED:

None

**FOREIGN APPLICATIONS VERIFIED:

JAPA 2000-393417 12/27/2000

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PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	ATTORNEY DOCKET NO
Foreign priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no		33035M084	
35 USC 119 conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no			
Verified and Acknowledged Examiners' initials			
TITLE : Heterojunction bipolar transistor and method of making heterojunction bipolar transistor			

U.S. DEPT. OF COMM./PAT. & TM-PTO-436 (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Paul E Brock II Assistant Examiner		CLASSES ALLOWED	
ISSUE FEE		1. Invention		Total Claims	10
Amount Due	Date Paid	Primary Examiner		Print Claim for	0.8
<input type="checkbox"/> TERMINAL DISCLAIMER		3-30-04 PREPARED FOR ISSUE		DRAWING	1
				Sheets Drawn	11
				Figs. Drawn	25
				Print Figs.	8A, 1F
				Application Examiner	3/30/04
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